AIP | Applied Physics Letters

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Citation: Appl. Phys. Lett. **100**, 093305 (2012); doi: 10.1063/1.3691181
View online: http://dx.doi.org/10.1063/1.3691181
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v100/i9
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Ultra-low voltage, organic thin film transistors fabricated on plastic substrates by a highly reproducible process

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(Received 24 November 2011; accepted 9 February 2012; published online 1 March 2012)

Organic thin film transistors have been fabricated on plastic substrates using a combination of two ultrathin insulating films, namely a 6 nm Al_2O_3 film (grown by UV-Ozone treatment of a pre-deposited aluminium film) and a 25 nm parylene C film deposited by vapour phase, as gate dielectric. They show a very low leakage current density, around 2×10^{-9} A/cm^2, and, most importantly, can be operated at voltages below 1 V. We demonstrate that this low-cost technique is highly reproducible and represents a step forward for the routine fabrication of ultra-low voltage plastic electronics. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3691181]

Organic electronics is under the lens of scientific and technological investigations since conductive polymers were first introduced in 1977 by Shirakawa *et al.*,[1] later awarded with the Nobel Prize for Chemistry. In particular, the first example of organic thin film transistor (OTFT) was introduced by Koezuka *et al.* in 1983 (Ref. 2) giving rise to a whole new branch of scientific literature on devices that are performing progressively better[3–5] and enabling very interesting applications in several fields.[6–9]

Unfortunately, the very high voltages normally needed for biasing OTFTs pose a serious concern for many applications. In fact, it is virtually impossible to battery-operate OTFTs without a suitable electronic (non organic) interface for step-up conversion of the battery supply voltage. A brilliant solution to this problem was proposed in 2000 by Collet *et al.*[10] who first introduced the use of self assembled monolayers (SAMs) for realizing the gate dielectric of the transistor. Halik *et al.* in 2004 (Ref. 11) further improved these first results, demonstrating that by realizing a high quality SAM on silicon dioxide, also the gate leakage through the SAM may be lowered by several orders of magnitude. Finally, Klauk *et al.*[12] in 2007 were able to obtain a good insulating layer from SAMs deposited on a metal oxide that can be obtained at low temperature on flexible (plastic) substrates, i.e., they demonstrated that the packing density of SAMs on metal oxides may be high enough to obtain a dielectric layer with a very low leakage current and the desired surface properties for optimizing the dielectric/semiconductor interface. However, the efficiency of the dielectric layer is dependent on the quality of the SAM which is strongly affected by several parameters as substrate surface corrugation and environmental conditions, as temperature and humidity.[13,14]

Other interesting solutions for lowering bias voltages of OTFTs have been proposed by several authors using high-k materials;[15,16] in these cases, the gate dielectric capacitance was increased by increasing its dielectric constant, thus allowing a thicker layer to be employed. However, these fabrication procedures are not suited for application on the majority of plastic substrates as the processing temperature (300 °C) is close to the melting limits for such materials.

A very interesting solution was recently introduced by Ha *et al.*[17] who demonstrated that multilayer organic/inorganic self assembled nanodielectric (SAND) films, with average thicknesses from 5 to 12 nm, can be employed for the fabrication of low voltage OTFTs. Other very interesting approaches for the fabrication of thin insulating films from liquid phase have been also introduced, such as the use of cross-linked polymer blends.[18] Recently, Cheng *et al.*[19] reported on a novel approach for the fabrication of cross linked Cytop ultrathin insulating films. These results are promising, but for achieving large capacitances, it is necessary to employ ultralow thicknesses that can be achieved basically only by spin-coating on limited areas; very recently, Murphy *et al.*[20] introduced bar coating as a promising tool for obtaining polymeric thin films with thickness below 100 nm over large areas thus opening interesting perspectives also for low voltage devices. Finally, electrolyte gated transistors that can be fabricated on flexible plastic substrates, with very easy and cost-efficient techniques, have also been demonstrated as a valuable solution for the realization of low voltage transistors.[21–23] Though very interesting, this approach suffers the strong limit that, in order to be operated, the electrolyte should not exchange charge with the organic semiconductor and this is not always necessarily the case; moreover, switching speeds could be severely limited by ion diffusivity within the electrolyte.

In this paper, we propose an alternative fabrication procedure for obtaining an ultra-low voltage device that is simple, low-cost, and, most of all, very easily up-scalable to industrial size with a significant yield. These results have been achieved by employing a unique combination of different dielectric materials that are able to: (1) give rise to high values of gate capacitances; (2) create, at the same time, an efficient barrier to gate leakage and an optimal interface with the organic semiconductor, being this a key concept for optimizing the transistor performance.[24]

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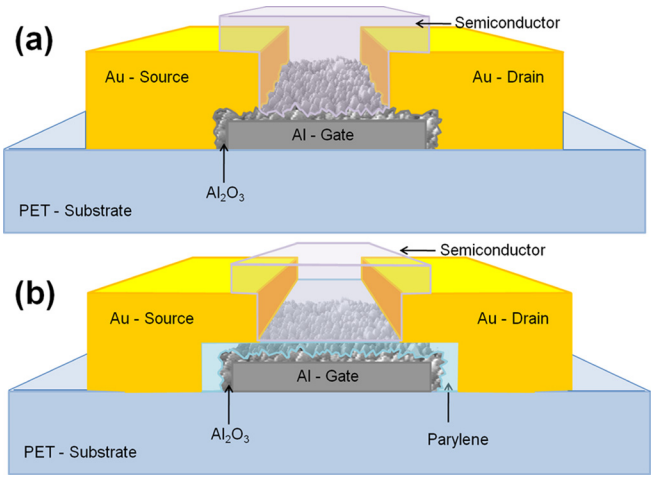

FIG. 1. (Color online) Schematic representation of OTFTs fabricated using a single, UV-Ozone grown, Al_2O_3 film (a) and a double layer configuration in which Par C is deposited on the previously grown Al_2O_3 film (b).

With this aim, we fabricated OTFTs on flexible polyethylene terephtalate (PET) films, using pentacene as organic semiconductor and a combination of Al_2O_3 and parylene C (Par C) as dielectric layer. OTFTs structures are all bottom-gate/bottom contact. The aluminum gate is deposited by thermal evaporation and patterned using a shadow mask. The Al_2O_3 layer is realized at room temperature by the means of UV-ozone oxidation (using a mercury lamp, UVP PenRay) performed in ambient conditions for a maximum time of 1 h. Parylene C is deposited by the mean of chemical vapor deposition (CVD) (specialty coating systems) at room temperature, using A174 as adhesion promoter. Thanks to the ease of the dielectric fabrication process, such a procedure can be very simply up-scaled to an industrial size. In fact, the employed procedure for Al_2O_3 growth can be performed at low costs over relatively large areas and, in addition, many other methods are available for aluminum oxidation.[12,25,26] On the other hand, even if parylene C deposition requires a dedicated instrumentation, it is already very widely employed in several industrial processes for the deposition of insulating films of different thicknesses (from tens of nm up to tens of μm) with excellent properties in terms of reproducibility and quality.[27,28]

Thermally evaporated gold source and drain contacts are realized on top of the Par C layer with a photolithographic process. A similar procedure was employed for realizing metal-insulator-metal (MIM) structures having an area of 2×2 mm^2. Pentacene was thermally evaporated at a base pressure of 10^{-6} Torr, whereas 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS) was deposited by drop casting from a 0.5% solution (in weight) using toluene as organic solvent. In the latter case, deposition was performed keeping the substrate at 60 °; after deposition, the film was annealed for 1 h at 80 °C.

Drain-source current (I_D) measurements were carried out at room temperature in air. An Agilent HP 4155 semiconductor parameter analyzer, provided with gold tips for contacting the electrodes, was used to control the gate voltage (V_G) and the drain-source voltage (V_D) and to measure I_D (the source being the common ground). For all devices, both mobility and threshold voltage were derived from the transfer characteristics in the saturation regime. Since the hysteresis was negligible for all devices, mobility and threshold voltage have the same value both in forward and backward gate voltage sweep.

Atomic force microscopy (AFM) measurements were obtained by means of a SPM SOLVER PRO by NT-MDT in semi-contact mode, using NSG01 tips. High resolution transmission electron microscopy (TEM) images were obtained using a FEI Tecnai F20 ST instrument.

We first fabricated devices based on a bare Al_2O_3 dielectric film (Fig. 1(a)) and carried out their complete characterization as thin film transistors. Different UV-ozone exposure times, from 10 to 60 min, have been tested, reaching, in the latter case, as demonstrated by TEM investigations reported in Fig. 2(a), a maximum thickness of around 6 nm (for a complete characterization of thickness vs. oxidation time see Fig. S1 in the supporting information, SI (Ref. 29)). Thanks to the very high gate dielectric capacitance (1 μF/cm^2),

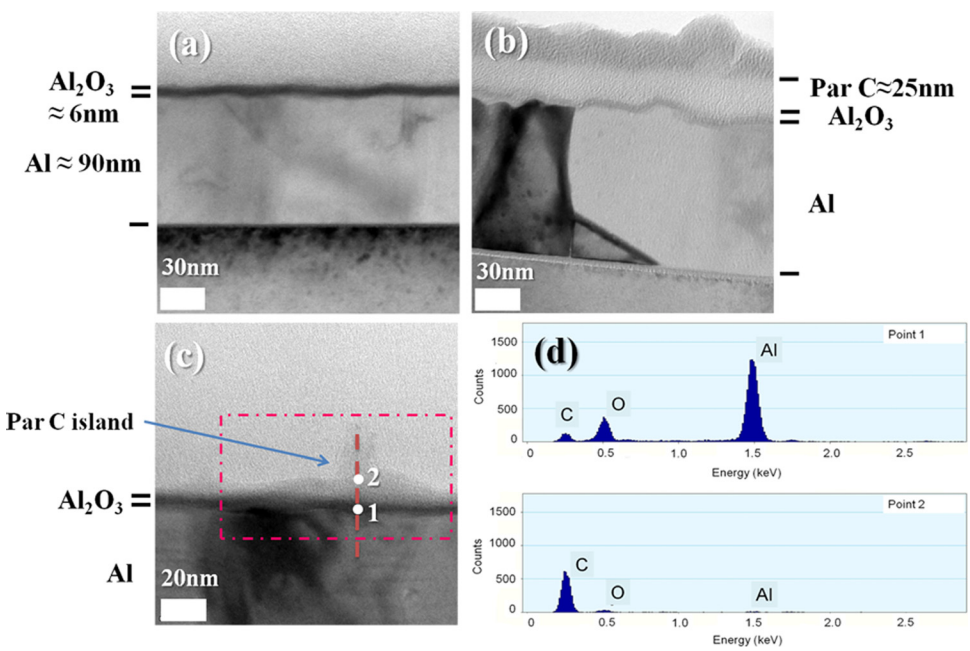

FIG. 2. (Color online) Transmission electron microscopy micrographs of (150 mg) Par C/Al_2O_3 (a) and (300 mg) Par C/Al_2O_3 (b) films; zoom on a Par C island in a (150 mg) Par C/Al_2O_3 sample (c). EDX spectra corresponding to points 1 and 2 in (c) showing the presence of a Par C island at the top of the Al_2O_3 film (d).

OTFTs assembled on the bare oxide show a very good field effect behavior and, most importantly, work with operating voltages lower than 2 V, with a threshold voltage usually around −1.2 V. However, very significant drawbacks were observed; in particular, a pronounced leakage current from gate to source, usually ranging around 6×10^{-6} A, with a vertical current density of 2.9×10^{-5} A/cm^2. Not less importantly, the final yield of the procedure is very low, ranging around 10%-15% of working devices (on several tens of devices). Moreover, these devices are also characterized by a very low carrier mobility (around 3×10^{-3}cm^2/Vs). A typical example of the electrical characteristics obtained using this configuration is shown in the SI, Fig. S2.[29] As revealed by AFM measurements, Al_2O_3 is characterized by a high surface corrugation with an average root mean square roughness (RMSR) higher than 5 nm. This feature strongly affects the morphology of the deposited pentacene film, which is characterized, as shown in Fig. 3(a), by pronounced granular structure with average domains dimensions of around 100 nm.

In order to improve the device characteristics, we deposited (by CVD) a second, very thin, parylene C film on the previously grown Al_2O_3 film; the schematic representation of the structure is shown in Fig. 1(b). The goal of this procedure was, on the one hand, a "sealing" of the leakage paths across the oxide without a significant decrease of the dielectric capacitance, and, on the other hand, an improvement of the interface with the organic semiconductor, since, as several times reported in the literature,[12,30] Al_2O_3 usually does not give rise to an ideal interface with the organic semiconductor. Parylene C has been chosen for its favorable dielectric and structural properties,[31] for its robustness in comparison with other passivation layers[32] and also because it can be deposited by CVD, a technique that allows to achieve a very good control on the deposition of very thin films over large areas, independently of the substrate quality. This aspect is particularly important for aiming at the industrial scalability of the proposed fabrication procedure.

Different amounts of Par C have been employed in this investigation, starting from 30 mg up to 300 mg, in order to achieve the best performances in terms of process yield, and the most favorable electrical properties of the gate dielectric film in terms of capacitance and vertical resistance, as shown in Fig. 4. By combining information coming from TEM and the electrical characterization of the MIM structures, we argue that Par C initially penetrates among the oxide grains and then starts forming an overlayer. Figure 2 shows the comparison between a sample with an oxide layer onto which 150 mg of Par C have been deposited (Figs. 2(a) and 2(c)) and one with 300 mg of Par C (Fig. 2(b)). While in the latter case the layer of Par C is clearly distinguishable (and has a thickness of 25 nm), this is not the case for the former structure (and for devices with even smaller amounts, data not shown): apparently, only oxide is visible (with a thickness of about 6 nm). Occasionally (Fig. 2(c)), it is possible to observe, on top of the oxide, small islands that, analyzed by Energy Dispersive X-Ray Spectroscopy (EDX) (Fig. 2(d)), are rich in Carbon (in comparison with the underlying oxide layer), and are, therefore, attributed to Par C. Thus, it is clear that the amount of Par C, in this case, is not sufficient to form a continuous film. However, the electrical analysis of MIM structures (results reported in Fig. 4), clearly demonstrates that both capacitance and vertical resistance are significantly affected when such an amount of Par C is deposited on top of the oxide: the leakage is reduced of more than 2 orders of magnitude, while the capacitance decreases of a factor 5 (with respect to bare Al_2O_3). Both these data support the idea that Par C penetrates among the oxide grains, sealing the leakage pathways across the oxide, and reducing the global dielectric constant of the derived "metamaterial". In addition, AFM reveals that the Par C film acts as a smoothing layer, allowing a dramatic reduction of the surface corrugation, with a RMSR that goes from 5.5 nm for Al_2O_3 films to 1.3 nm for Par C (300 mg)/Al_2O_3 films. Correspondingly (Figs. 3(a) and 3(b)), a clear increase of the average grain dimension of pentacene is observed (from around 100 nm to 500 nm).

We observed, by TEM investigations (see Fig. 2(b)), that 300 mg of Par C form a complete and almost uniform film, with an average thickness of 25 nm; thus, this value realistically represents the minimum thickness for achieving a good trade-off between gate dielectric capacitance and vertical resistance (see Fig. 4). Clearly, the correspondence

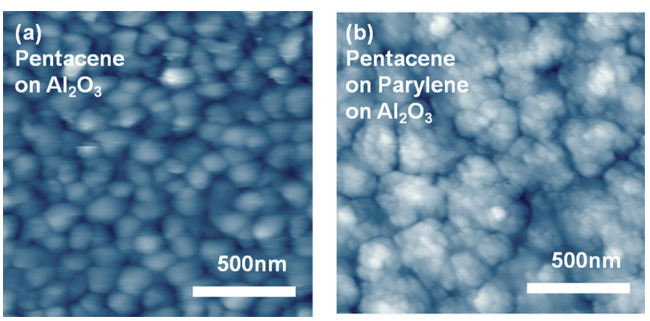

FIG. 3. (Color online) Atomic force microscopy micrographs of pentacene deposited on bare Al_2O_3 (a) and pentacene deposited on (300 mg) Par C/Al_2O_3 (b). Al_2O_3 and (300 mg) Par C/Al_2O_3 (data not shown) are characterized by a RMSR of 5.5 nm and 1.3 nm, respectively. As a consequence, the average dimensions of pentacene domains are significantly different in the two cases, namely 100 nm (a) and 500 nm (b).

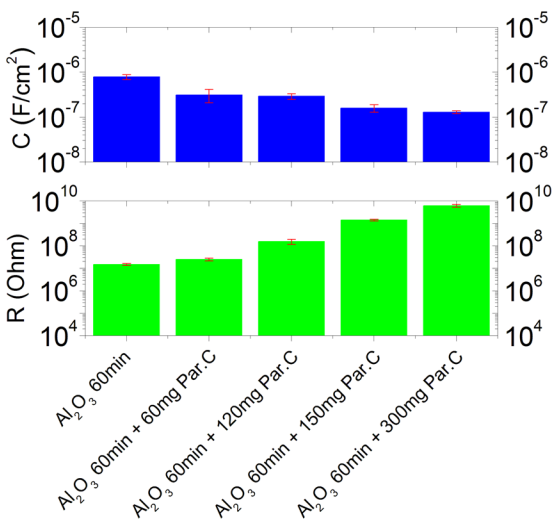

FIG. 4. (Color online) Vertical resistance and capacitance values of MIM structures based on different combinations of Par C and Al_2O_3

between the amount of dimer and the thickness of the film depends on the features of the CVD chamber and a calibration should be done for each coating equipment. The electrical characterization of OTFTs fabricated using this technique showed a dramatic improvement of all the most meaningful parameters. First of all, as can be noticed from Figs. 5(a) and 5(b), the fabricated devices show a maximum mobility around 6×10^{-2} cm^2/Vs, and, most importantly can be operated at very low voltages, as they are characterized by a very low value of the average threshold voltage (−0.5 V), even lower than in devices based on bare Al_2O_3, despite the lower gate dielectric capacitance. This is particularly important as it demonstrates that for achieving low operating voltages, it is crucial to have a proper control of interfacial properties of the dielectric layer, in addition to a high value of the gate dielectric capacitance. Another important parameter, directly linked to the quality of the dielectric/semiconductor interface, is the subthreshold slope (S), extracted from the transfer characteristics, from which the maximum density of interfacial trap sites can be derived,[33] $N_{SS}^{\max} = \left[\frac{S \cdot \log(e)}{kT/q} - 1\right] \frac{C_i}{q}$. In this case, we obtained an average S of 350 mV/dec, that leads to $N_{SS}^{\max} = 4 \times 10^{12}\,\text{cm}^{-2}\,\text{eV}^{-1}$ (i.e., almost two orders of magnitude lower than in devices assembled on bare Al_2O_3, see Table I in SI (Ref. 29)). The obtained S values are slightly higher compared to other cases reported in the literature[11,12,34] but, in our structures, the capacitance is almost 5 times smaller. This means that the maximum density of trap sites in our case is lower. Compared to more recent results,[35] S is lower, but $N_{SS}^{\max}$ is of the same order of magnitude. Moreover, we obtained a breakdown voltage higher than 5 MV/cm, and most importantly, a very low leakage current density (more than 4 orders of magnitude smaller than in bare Al_2O_3 devices, i.e., around 2×10^{-9} A/cm^2 recorded at 0.66 MV/cm) correlated with a remarkable increase of the process yield up to 90% (over hundreds of fabricated devices). All devices were fabricated on commercial PET plastic substrates employed as received. These substrates, as shown in Fig. S4,[29] are usually characterized by very pronounced surface defects that can cause severe irregularities or even breaks across the gate dielectric leading to a failure of the device. A proper planarization process, as suggested by Sekitani *et al.*[34] for SAM based devices, could certainly significantly improve this yield.

A statistical analysis of the most meaningful electrical parameters is reported in Table I in the SI. It is worth noting that, despite an improvement of one order of magnitude compared to bare Al_2O_3, the achieved mobility is still smaller than the average mobility reported in the literature for pentacene based devices.[11,12,34] As a matter of fact, pentacene growth is very sensitive to the surface corrugation of the substrate and high mobilities can be achieved only by employing insulating films with an average roughness much smaller than 1 nm. Again, the use of a planarization layer on the plastic substrate[34] or the employment of organic semiconductors that are much less sensitive to the substrate corrugation[36] could certainly be beneficial for the device performance. It is noteworthy that when a less substrate-sensitive semiconductor, i.e., TIPS-pentacene, was employed, mobilities as high as 0.4 cm^2/Vs were achieved, with an average value of the subthreshold slope of around 200 mV/dec, (with the smallest achieved value of 70 mV/dec, corresponding to $N_{SS}^{\max} = 7.5 \times 10^{11}\,\text{cm}^{-2}\,\text{eV}^{-1}$). The typical output and transfer characteristics of TIPS based OTFTs are shown in Figs. 5(c) and 5(d).

Interestingly enough, OTFTs based on a single layer of Par C (with the same reported amounts but without Al_2O_3) have been also tentatively fabricated and tested, but working devices were never obtained, as the leakage currents were always too high. This is particularly important as it demonstrates that the two single dielectric films cannot be employed alone for the fabrication of efficient ultra-low voltage devices, whereas a proper combination of the two gives rise to devices with optimal performances. In conclusion, we have demonstrated the potentiality of a combination of a metal oxide (namely Al_2O_3 but the technique may in principle be applied to any metal oxide) and of the organic

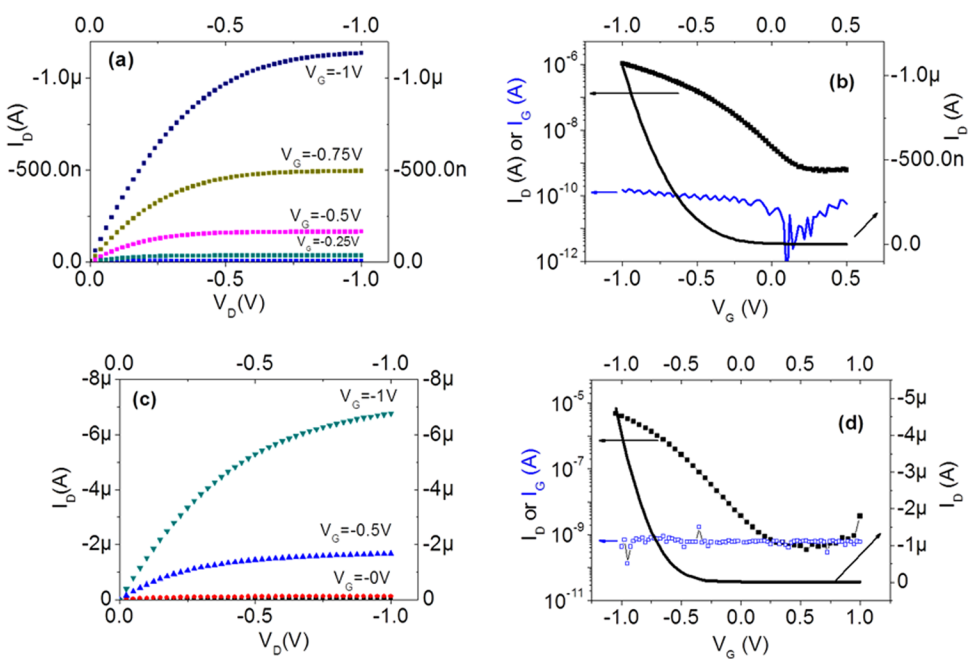

FIG. 5. (Color online) Output and transfer characteristics of pentacene ((a) and (b)) and TIPS-pentacene ((c) and (d)) OTFTs fabricated using a double layer Par C/Al_2O_3. The transfer characteristics have been recorded in the saturation regime at $V_{DS} = -1$ V.

dielectric parylene C, for the routine realization of ultra-low voltage organic thin film transistors. With this combination of dielectric materials, we have obtained devices that: (a) work with bias voltages of 1 V and have an average threshold voltage of −0.5 V; (b) within their working voltage range do not show any significant leakage. We have also demonstrated that this technique is able to give rise to a process yield of more than 90% in non-optimized conditions and, therefore, has a very interesting potential in terms of industrial scalability.

The authors would like to thank Beatrice Fraboni and Silvia Milita for fruitful discussions on the results; Roberto Balboni and Jacques Legeleux for helping with TEM/SEM investigations. Finally, the authors acknowledge financial support by the European Commission, under the VII FP Project "Roboskin," Contract Number 231500. P. Cosseddu acknowledges Regione Autonoma della Sardegna (RAS) for funding his research activity under the POR Sardegna FSE 2007-2013, L.R.7/2007 CRP Prot. No. 1399/207. S. Lai acknowledges Regione Autonoma della Sardegna (RAS) for funding his Ph.D. activity under the POR Sardegna FSE 2007-2013.

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