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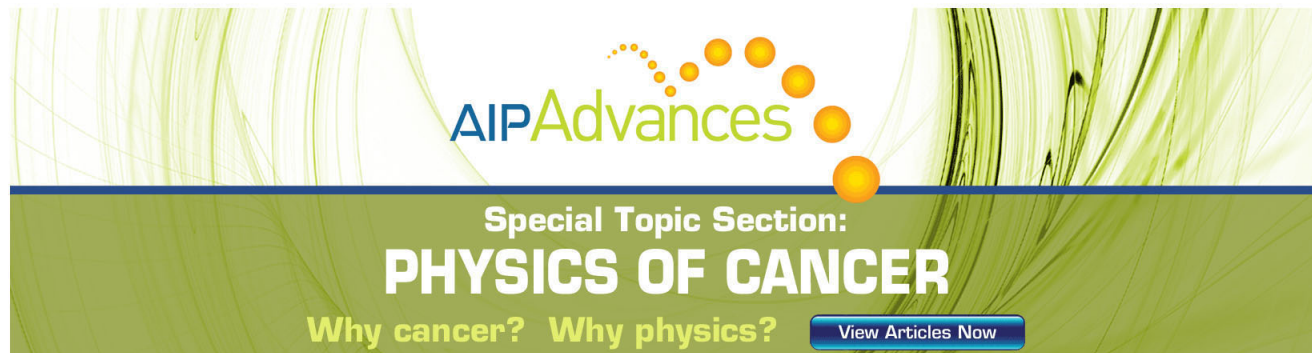Journal Homepage: http://apl.aip.org/
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Conductive atomic force microscopy studies on dielectric breakdown behavior of ultrathin Al$_2$O$_3$ films

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Ultrathin films of Al$_2$O$_3$ prepared by atomic layer deposition have been subjected to local electrical stress analysis using conducting atomic force microscopy. The loss of local dielectric integrity through current leakage in these extremely thin films is studied using scanning spreading resistance imaging. Our experimental results shows that repeated voltage stress progressively increases number of leakage spots. While the density of leakage spots increase with higher applied bias for thin oxide films, initial increase and reduction in leakage spots are observed for thick films. © *2011 American Institute of Physics*. [doi:10.1063/1.3560307]

The electrical degradation and dielectric breakdown (BD) of ultrathin oxide films are one of the major concerns for the reliability of metal oxide semiconductor (MOS) field effect transistor in ultra large scale integration.[1] Considerably large efforts have been dedicated to understand the physics behind oxide degradation and BD characteristics. Currently, intensive research is being carried out by many groups in search of high-k dielectric material to replace the existing SiO$_2$ whose leakage current reach beyond acceptable limits due to continuous downscaling of the MOS devices. The potential candidate to replace SiO$_2$ should meet very stringent specifications with an equivalent oxide thickness of less than 1 nm with increased gate capacitance and without compromising leakage currents.[2] To achieve these objectives, ultrathin high quality gate insulators with higher dielectric constant, improved structural and physical parameters are required to limit the leakage current. In these aspects, we consider Al$_2$O$_3$ as one of the promising candidates as a gate insulator due to its excellent low leakage current density, large band gap (8.8 eV), higher dielectric constant (9–10), thermal, and chemical stability. Although thin film of Al$_2$O$_3$ posses lower band gap[3–5] than its bulk counterpart, it finds many technological applications. In this letter, we examine current leakage behavior of extremely thin Al$_2$O$_3$ oxide film (0.4–2 nm) on silicon substrate with progressive electrical stressing and I–V measurements.

For the current investigation, ultrathin films of Al$_2$O$_3$ are prepared using atomic layer deposition (ALD) technique and the details are discussed elsewhere.[6] 1 and 5 cycles of Al$_2$O$_3$ thin films are deposited on n-Si (4–6 Ω cm) with each cycle of reaction results in 0.4 nm film thickness. The samples are labeled as ALD1 and ALD5 with nominal thickness of 0.4 nm and 2 nm, respectively.

The electrical characterization of these samples is carried out using AFM (Solver Pro, M/S NT-MDT, Russia) techniques which differs substantially from conventional methods. Unlike traditional techniques which provide spatially averaged information of the microscopic phenomenon, conductive atomic force microscopy (C-AFM) allows us to characterize the dielectric film both topographically and electrically with nanometer resolution. Using constant bias mode, we have mapped a few cursory current images on samples ALD1 and ALD5. This simultaneously acquired topographic and scanning spreading resistance imaging maps give information on surface roughness and current contrast. We observe that the topography of the image is smooth without any features. However, the current image exhibit few isolated bright spots suggesting current conduction through leakage paths.[7] To monitor and improve statistics on the number of these leakage paths, images are recorded at different areas on samples ALD1 and ALD5. The bright spots in the current image appear due to low level leakage current under high electric field and popularly known as stress induced leakage current (SILC).[8] Knowledge on the current intensity distribution n(I) on the entire image can provide a direct account on the dielectric integrity of this stressed region. Hence, based on these images the current intensity distribution is studied by constructing a histogram from current values of each pixel with bin size of 1.53 pA as shown in Fig. 1.
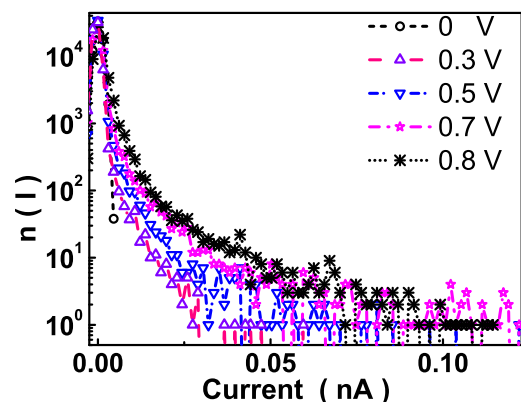

FIG. 1. (Color online) Histograms constructed from the pixel values of current on acquired images at different bias conditions for the sample ALD1.

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FIG. 2. (Color online) Current images at different biases for sample ALD1 (a) 0.2 V, (b) 0.4 V, (c) 0.8 V (scan area 500×500 nm^2), and (d) 0.8V (scan area 1000×1000 nm^2). The inner stressed area of 500×500 nm^2 shows large current leakage spots in comparison to the outer area (unstressed).
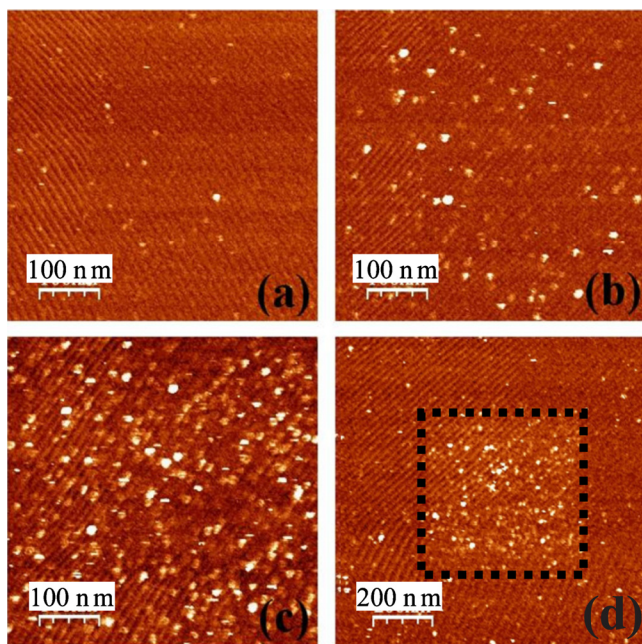

FIG. 3. (Color online) Current images at different biases for sample ALD5 (a) 0.4 V, (b) 0.8 V, (c) 1.2 V (scan area 500×500 nm^2), and (d) 1.2 V (scan area 1000×1000 nm^2). The inner stressed area of 500×500 nm^2 show reduction in current spots in comparison to the outer area (unstressed).

From this histogram it is evident that the statistical distribution peaks at low current values. A systematic increase in the number of leakage spots with bias voltage can be seen. The peaking of current intensity at very low current values confirms the stressing is only moderate and conduction is due to leakage currents and not by BD. The negative current in the histogram is attributed to the offset in the current amplifier and it also manifest as background strips in the current image. Having obtained and verified the range of stress field for inducing leakage currents, we further mapped current images on a fresh region to study the impact of electrical stress on the charge conduction and trapping in the dielectric film. Sequence of images are acquired using constant bias over a specific region and for each image, we choose to increment the bias in steps, in the range 0–1.2 V on sample ALD1, to study the dynamics of degradation as shown in Fig. 2. These images illustrate the effect of cumulative electrical stress over 500×500 nm^2 as shown in Figs. 2(a)–2(c). To understand the extent of electrical stress, we also performed a 1000×1000 nm^2 scan encompassing the previously stressed 500×500 nm^2 region as shown in Fig. 2(d). During this larger scan, proper precaution is taken to maintain the scan velocity compatible to the previous scans to remove any ambiguity that could arise due to time dependent stressing. Figure 2(d) shows the pronounced distinction between the cumulative effect of electrically stressed region (indicated by a boundary) from the less stressed region around it. We understand that during repeated scans over a specific region, electrons are injected from the AFM tip into the oxide conduction band and release their energy near the anode to possibly break the bonds of Al_2O_3 at local regions which results in creation of traps. Sakakibura *et al.*,[9] have found that the generation of trap density increases with an increase in the stress field. In the case of higher stress fields, a large number of traps are generated as oxide thickness is reduced.[10] The den-
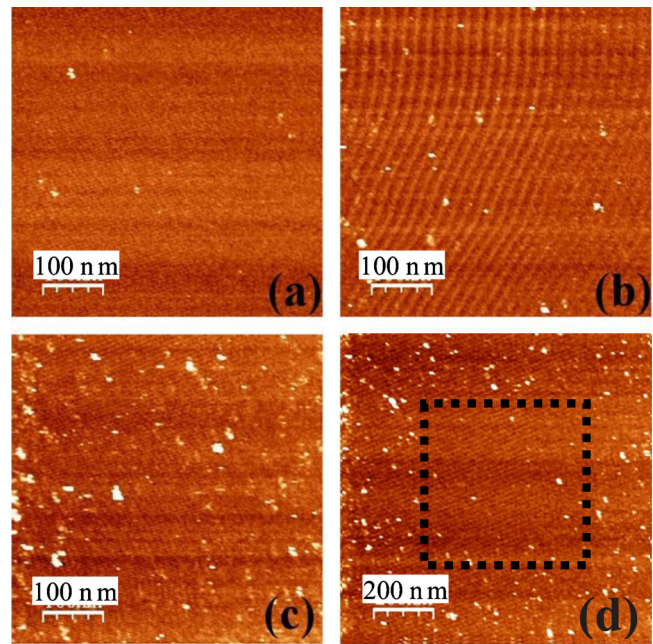
sity of leakage spots in the stressed region can also be used as a measure of dielectric integrity.

Figure 3 shows the current images acquired at different applied biases ranging from 0.4–1.2 V on sample ALD5. Figure 3(a) shows the current contrast with a few bright spots at initial bias voltages and the density of leakage spots continue to show an upward trend as in the case of ALD1. At this juncture a large area scan of 1000×1000 nm^2 is used as in the previous case to compare the variation in density of leakage spots with unstressed region. However, we note that the increasing trend in the leakage spots does not sustain as expected but started diminishing beyond 1.2 V bias. In order to confirm this observation, a current intensity histogram is constructed as in the earlier analysis and shown in Fig. 4. By a careful study of this histogram we could derive a few interesting results. First, the dielectric integrity can be found intact since the current intensity distribution peaks at very low current. However, a gradual increase in the density of leakage spots could be observed with increasing bias upto
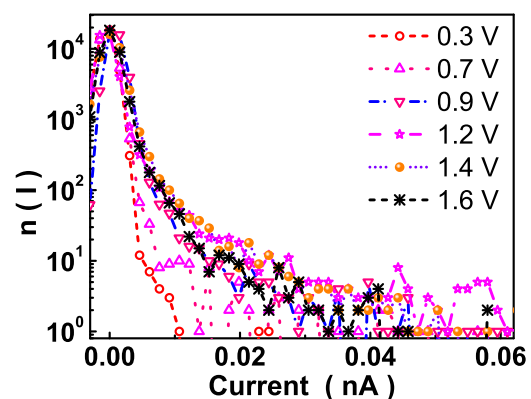

FIG. 4. (Color online) Histograms constructed from the pixel values of current on acquired images at different bias conditions for the sample ALD5.
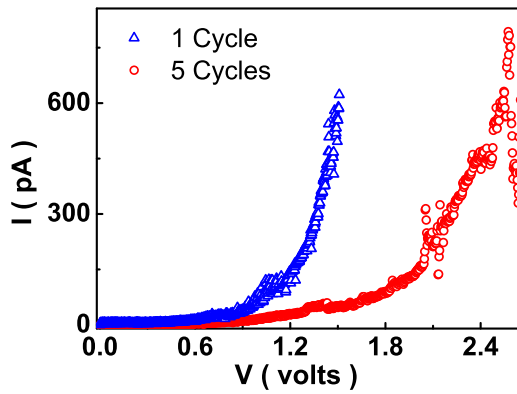
FIG. 5. (Color online) Typical I-V curves for the samples ALD1 and ALD5, showing oscillations in the current due to trapping and detrapping.

0.9 V. For 1.2 V bias, the number of high intensity spots increases remarkably, with a fall at the lower intensity spots. However, this increasing trend is found to get reversed at the bias of 1.6 V as can be seen from Fig. 4. This observation also reflects in the central square of Fig. 3(d) which indicates that the stressed region is relatively quite with reduction in density of spots than the region around it. To further investigate this seemingly anomalous behavior, we resolve to perform I-V measurements for some possible clues.

Figure 5 shows the I-V curves made at different regions of the specimen. A voltage ramp is applied with step size of 5 mV at a ramp rate of 1 V/s. This technique enables quick determination of an oxide's intrinsic reliability and also provides information on defects. The I-V curves fit well with direct tunneling model as expected for the case of thin films below 3 nm thickness.[11] The current flow in direct tunneling mechanism can be written as,[12]

$$I_{dir} = A_G A t_{ox}^2 \exp\left\{ \frac{-B[1-(1-qV_{ox}/\Phi_B)^{1.5}]}{t_{ox}} \right\}, \quad (1)$$

where $A=(q^3(m/m_{ox})/8\pi h\Phi_B)$, $B=(8\pi\sqrt{2m_{ox}\Phi_B^3}/3qh)$, oxide potential $V_{ox}=V_G-V_{FB}-\phi_s$, A_G is the contact area, t_{ox} is the effective oxide thickness, m_{ox} is the effective electron mass in the oxide, Φ_B is the barrier height at the Si-oxide interface, V_G is the Gate voltage, and V_{FB} is the flat band voltage. For fitting I–V measurements, the parameters in the Eq. (1), A_G, m_{ox}, and Φ_B are taken as 500 nm^2, $0.35m_0$, and 3.25 eV, respectively. The estimated thickness for ALD1 and ALD5 are about 1.5 nm and 2 nm, respectively. We also repeated the above measurements in dry N_2 atmosphere for any possible clues on ambient effects. While we found the N_2 atmosphere helps in reduction in adsorbed moisture to improve the longevity of the tips, the results remain the same. Further, the calculated oxide thickness depends not only on the physical thickness but also on the electrical properties of the oxides. Noticeable oscillations in the current indicate trapping and detrapping of charges in the dielectric film.[13] By calculating the derivative, the sharp deviation in the current versus voltage slope can be identified as the onset of BD and can be seen to occur at 0.8 and 2 V for samples ALD1 and ALD5, respectively. The estimated BD field for these films, ALD1 and ALD5, are found to be about 20 MV/cm and 10 MV/cm, respectively.

We note that the stress induced electrical degradation of film ALD1 is remarkably different from ALD5, although, these two differ only in their thickness. In the sample ALD1,

the SILC increases with bias voltage. This process can be better understood by percolation model. According to this model, the increase in current with voltage is due to the formation of percolation paths upon continuous generation of electron traps. Once the density of traps reach certain critical value, more percolation paths are formed resulting in a significant increase in conductivity.[14,15] On the other hand in the films ALD5, the SILC increases with voltage under low bias condition and then reduces at higher bias. The reduction in current with higher bias is due to the negative charge trap in the stress induced defects in the oxide film.[16] The creation of such defects under high electric field stress is an inherent phenomenon in the dielectric. These defects capture the electrons injected by the tip into the oxide and create an electric field that opposes further injection of electrons. This process manifests as an injection barrier and accounts for the reduction in current conduction. We believe that this effect is intimately connected to a critical film thickness. We also realize the existing percolation models do not have a parameter that depends on this process. This type of behavior is evidenced earlier for 5–6 nm thick SiO_2 dielectrics.[17]

In conclusion, we have investigated the SILC in ALD grown ultrathin Al_2O_3 films using C-AFM. Our result shows, the SILC and degradation of thick film (>1 nm) differ significantly from thin film due to formation of injection barrier. The current oscillations in the I–V measurement are found large for thick films due to charge trapping and detrapping. The low SILC is an encouraging aspect of this material to employ as a gate dielectric with BD field as high as 20 MV/cm.

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