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New method of creation of a rearrangeable local Coulomb potential profile and its application for investigations of local conductivity of InAs nanowires

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ABSTRACT

We present a new technique to create a reconfigurable Coulomb potential profile. The potential profile on the sample surface covered with residual polymethyl methacrylate (PMMA) layer as charge accumulation substance is performed with a low DC voltage applied to conductive probe tip of scanning microscope. To characterize the resulted Coulomb potential profile Kelvin probe technique is used. The effectiveness of this method is demonstrated by performing measurements of the local conductivity of InAs quantum wires. These investigations revealed an inhomogeneous conductivity of the wires and the formation of a potential barrier in the wire at the contact pad interface when the electronic system of the wire is depleted.

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1. Introduction

In addition to standard method to create and configure low-dimensional structures such as lithographically defined gates or mesas there are also methods using a tip of a scanning probe microscope. The latter approach can be divided into two subclasses. The first one includes ‘irreversible techniques’ such as oxidation of GaAs/AlGaAs heterostructure [1], Ti film [2] and graphene [3] or irreversible mechanical or electrical destruction of structure with scanning probe [4]. The second class comprises ‘reversible techniques’ including reversible mechanical deformation with atomic-force microscope (AFM) tip [5] or creation of erasable Coulomb potential [6,7]. It is possible to include scanning gate imaging [12–15] in the ‘reversible techniques’ list.

Scanning gate microscopy is a very powerful method especially if the position of the object under investigation such as defect in quantum wire or chirality changing junction in carbon nanotubes is not well defined initially and it is not possible to make precise configuration of the side gates to articulate locally the density of electrons in one-dimensional (1D) sample. On the other hand it is not possible to create complex Coulomb potential profile using the single charged tip. So more flexible technique involving charge accumulation layer such as polymethyl methacrylate (PMMA) and conductive probe for precision manipulation with accumulated charges is required. This technique must not

destroy the 1D sample under investigation mechanically or electrically as well.

Several papers are dedicated to the study of different types of polymethyl methacrylate (PMMA) charging with scanning probe facilities [7–9]. However, no effective application of this promising method of configuration of the Coulomb potential for investigations of the local conductivity of 1D structures has been published, yet.

In present paper we introduce a new method to create a reconfigurable local Coulomb potential using PMMA as a charge accumulation layer and demonstrate its application for investigations of the local conductivity of 1D samples. We use a residual PMMA layer covering the sample surface with a thickness of 7–10 nm [10,11] comparable to radius of the probe tip and taking into account the provisional high resolution of the resulted potential profile [8]. The measurement of the thickness of the resulted PMMA layer was performed by scratching the layer with AFM tip and measuring the resulted profile. Charging is made by contact emission employing a conductive scanning probe microscope tip and applying a low (less than 5 V) DC tip voltage. Charging was performed in tapping mode of the microscope. These conditions allow to eliminate any sample damaging during charging. Previously two different methods were used to charge a PMMA layer [7–9]: (1) a non-contact AFM mode with a Corona discharge method where a high voltage of tens of volts was applied to the tip; (2) a direct charging using contact mode of the AFM. Both methods are not as safe as the one presented here because of the high voltage applied to the tip (method 1) and the contact mode of the AFM (method 2). The resulting Coulomb

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potential profile is quite stable in time even at room temperature, and the Kelvin probe technique is used for its mapping, similar to Refs. [7,8]. Our new method presented here was employed to investigate the local conductivity of 1D InAs nanowires [16–18].

2. Experimental

The undoped InAs nanowires used for our test measurements were fabricated using metal–organic vapor-phase epitaxy [19]. The diameters of the wires under investigation are in the range from 70 nm to 100 nm. The wires were placed on a n-type doped Si (1 0 0) wafer capped with a 100 nm thick SiO₂ insulating layer. The doped silicon substrate served as the back-gate to change the electronic density in the wire by applying back-gate voltage V_{BG} . The evaporated Ti/Au contacts to the wires and the markers of the search pattern were defined by electron-beam lithography [20,21]. The typical distances between the contact fingers are 2 μm .

All scanning experiments were performed using a commercially available scanning probe microscope P47 produced by NT-MDT. Topography mapping measurements and Coulomb potential profile configurations are done in tapping mode. The tip velocity during potential writing was fixed at 10 $\mu\text{m/s}$. We use a standard software for scanning probe lithography including raster and vector graphics to define the potential profile structures. The resulting Coulomb potential profile is subsequently mapped with Kelvin probe technique (see Ref. [15] for details). Electronic transport measurements on InAs nanowires are made with standard lock-in amplifier technique. An AC current of 10 nA is applied through the wire while the source-drain voltage is measured with the differential voltage amplifier of the lock-in amplifier. All measurements were performed at room temperature in air, i.e. at ambient conditions.

An example of application of the Kelvin probe technique to allocate the position of a defect in an InAs nanowire is presented in Fig. 1. A DC voltage of 0.8 V is applied in between source (top contact) and drain (bottom contact). The topography is shown in Fig. 1a. It is clearly visible that the wire is broken close to the drain contact pad. The image shown in Fig. 1b presents a Kelvin probe mapping of the same sample. A potential of 0.8 V is maintained along the wire up to the defect revealing its position in the wire similar to the topography measurements.

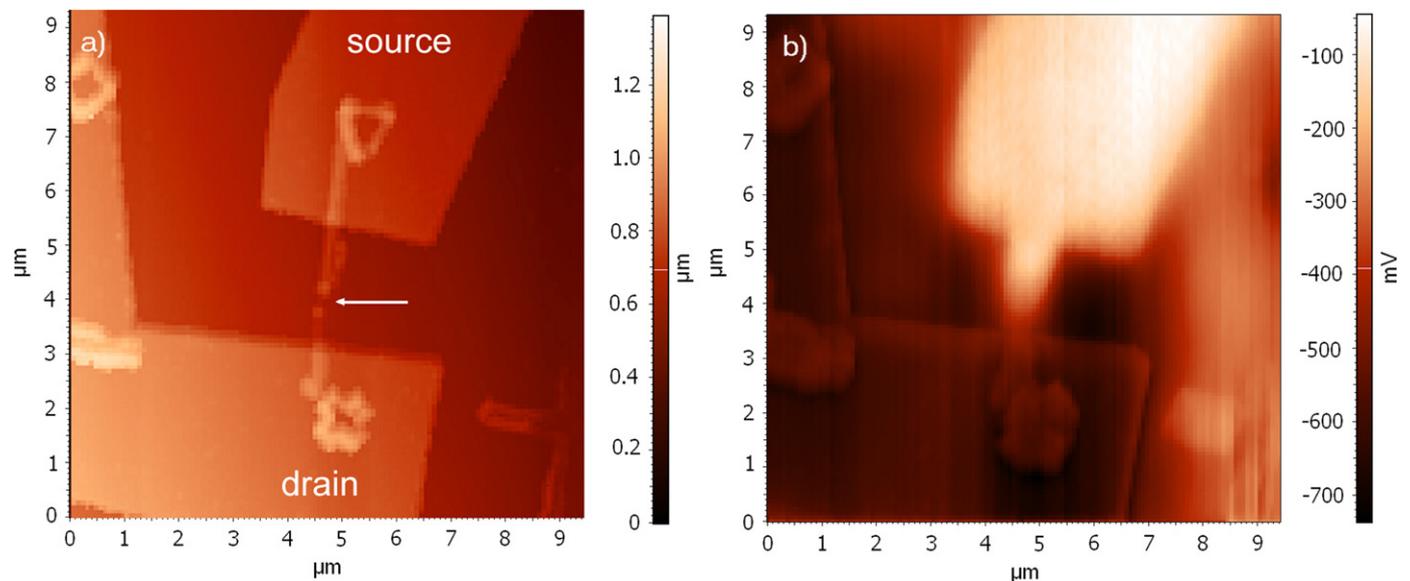


Fig. 1. Image (a) is a topography made by AFM of broken InAs wire. Image (b) presents Kelvin probe mapping of the area potential. Top contact (bright) is the source kept at potential of 0.8 V. The dark contact pad is drain kept to the ground, zero voltage is applied to the back-gate as well ($V_{BG} = 0$ V). Arrow points defect of the wire.

3. Results and discussion

In this section first the local charging of a PMMA layer will be demonstrated and characterized. Later on we will discuss how this method can be employed to modify the conductance in an InAs nanowire locally.

3.1. Local charging of a PMMA layer

To characterize our novel method of PMMA charging several step-like test structures were made with subsequent mapping of the resulting potential with Kelvin probe technique. An example of mapping of the step-like potential profile created with a charged AFM probe is presented in Fig. 2. The tip was swept a rectangle $5 \times 10 \mu\text{m}^2$ (in X direction tip was scanned 5 μm from $X = 2 \mu\text{m}$ to $X = 7 \mu\text{m}$) with a tip voltage of $V_t = +5$ V (Fig. 2a) and -5 V (Fig. 2b). The cross-sections of these two scans are shown in Fig. 3. Curves (a) dashed line and (b) solid line (both are shifted for clarity) are related to Fig. 2a and b, respectively. From the shape of the curves in Fig. 3, it is possible to conclude that this charging

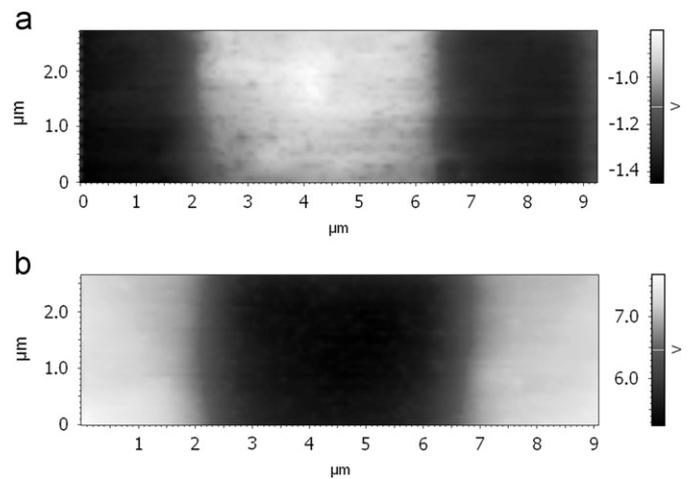


Fig. 2. Images (a) and (b) are Kelvin probe mapping of the potential of the surface performed after area scanning of the tip with tip voltage of +5 V and -5 V, respectively. Charged tip scans from $X = 2 \mu\text{m}$ to $X = 7 \mu\text{m}$.

technique is applicable to configure the local Coulomb potential profile with a deviation of profile of around 2 V. The achievable gradient of the potential profile is of 1 V/ μm .

It is worth noting that a single area or line scan with a charged tip does not produce a surface potential equal to V_t , see Fig. 2. The charging rather increases gradually from scan to scan, it means that a mapping of the real surface potential with Kelvin probe technique is necessary.

The resulting potential profile is not stable in time. The measurements of the potential redistribution with time are shown in Fig. 4. The scans shown in Fig. 4a–c are made 15 min, 1 h and 2 h after tip writing with $V_t = +5$ V, respectively. Fig. 5 shows a cross-sections of the images in Fig. 4a–c. This data reveals a time of 15 min for charge redistribution of structure of micron resolution (see Fig. 5). The potential redistribution is slow enough to be mapped and to perform a set of electronic transport measurements of the structure under investigation. One hour later the potential becomes almost flat (see Fig. 5). It is clearly visible that the induced charges diffuse with time increasing the potential of the nearby laying regions.

We made a calibration of the influence of the induced charges on the 1D structure such as an InAs nanowire as well. In Fig. 6a two dependencies of the InAs wire resistance after area scanning with $V_t = -1$ V (open circles) and with $V_t = -2$ V (open squares) vs back-gate voltage (V_{BG}) are presented. The surface potential according to Kelvin probe potential mapping is decreased after the second scan on -0.3 V. Both scans are performed by keeping

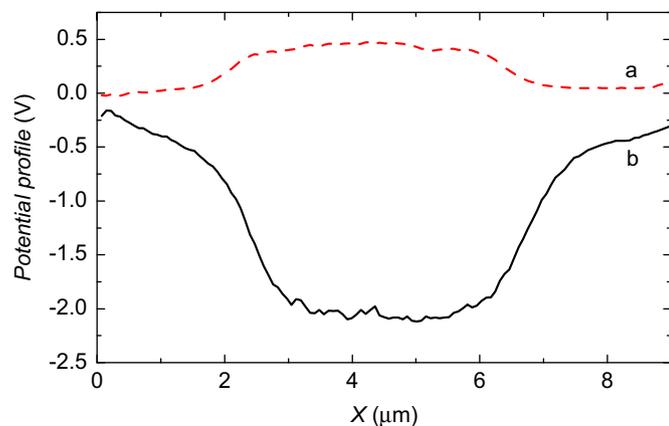


Fig. 3. Cut profile of Fig. 2(a) dashed line and (b) solid line (both are shifted for convenience). Charged tip scans from $X = 2$ μm to $X = 7$ μm .

the back-gate voltage $V_{BG} = 0$ V. The resistance of the wire at $V_{BG} = -1$ V after the first scan is equal to the resistance at $V_{BG} = 3$ V after the second scan, see Fig. 6a. It means that the mutual capacitance in between induced charges and the wire is approximately 13 times larger than the capacitance in between the wire and the back-gate ($C_{W-C}/C_{W-BG} \approx 13$) in case when the thickness of the SiO_2 insulating layer is of 100 nm only. Thus, we see that the induced potential alters the electronic system of the wire 13 times more effective than the back-gate and helps to set the electronic system under investigation in conditions unreachable using the back-gate only. The measured large value of the mutual capacitance (C_{W-C}) is reasonable taking into account the presence of the surface charge accumulation layer placed less than 10 nm beneath the surface of InAs wires [16,18], see Fig. 6b.

So, the introduced technique can perform deviation of the induced surface potential of around 2 V with decay time of 15 min. Taking into account that the mutual capacitance C_{W-C}/C_{W-BG} is of around 13 the introduced technique proves itself as a quite flexible tool. The achievable gradient of 1 V/ μm allows to use this technique to form structures with submicron sizes as well.

3.2. Local conductivity change in an InAs nanowire

Next we present two examples where our technique is employed to investigate peculiarities in the local conductivity of InAs wires. As it was mentioned previously our technique can be

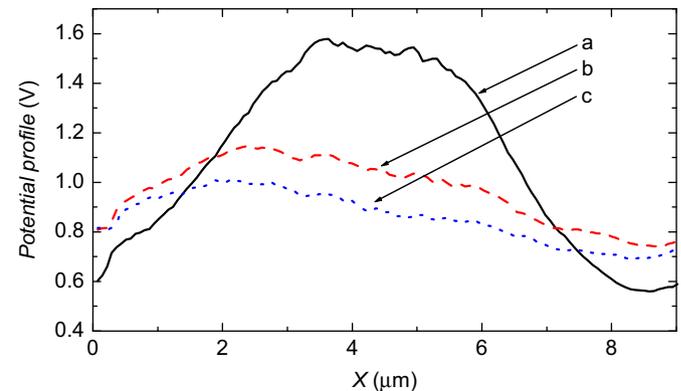


Fig. 5. Cut profile of Fig. 4(a) solid line, (b) dashed line and (c) dotted line. The established characteristic decay time is about 15 min.

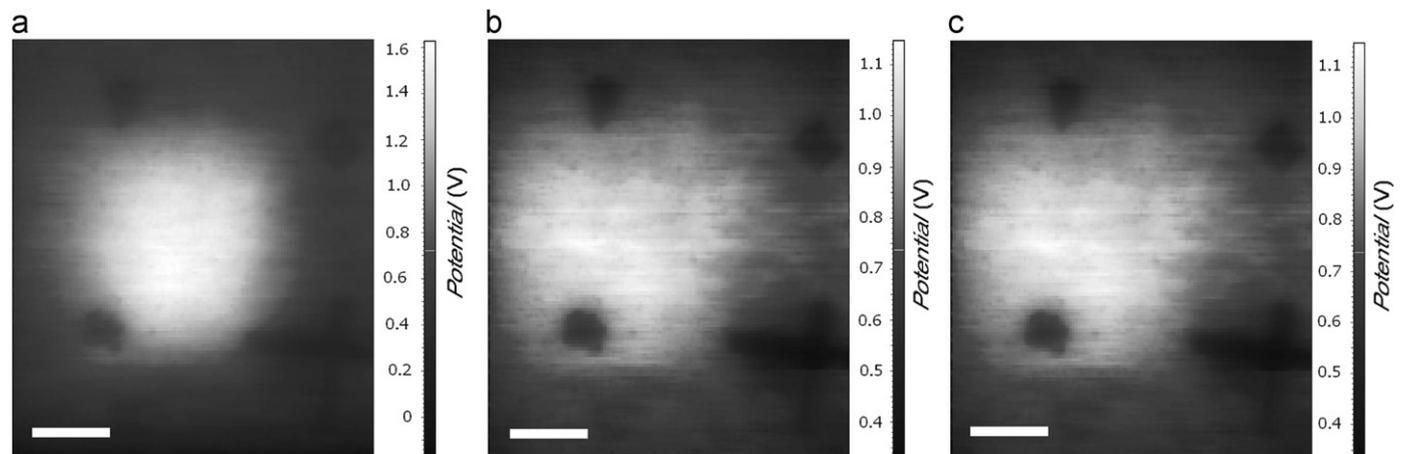


Fig. 4. Images from (a) to (c) are Kelvin probe mapping of the potential of the surface 15, 60 and 120 min later correspondingly after formation of the potential profile. The small dark spots on the scan are metallic markers. The scale bar is equal to 2 μm .

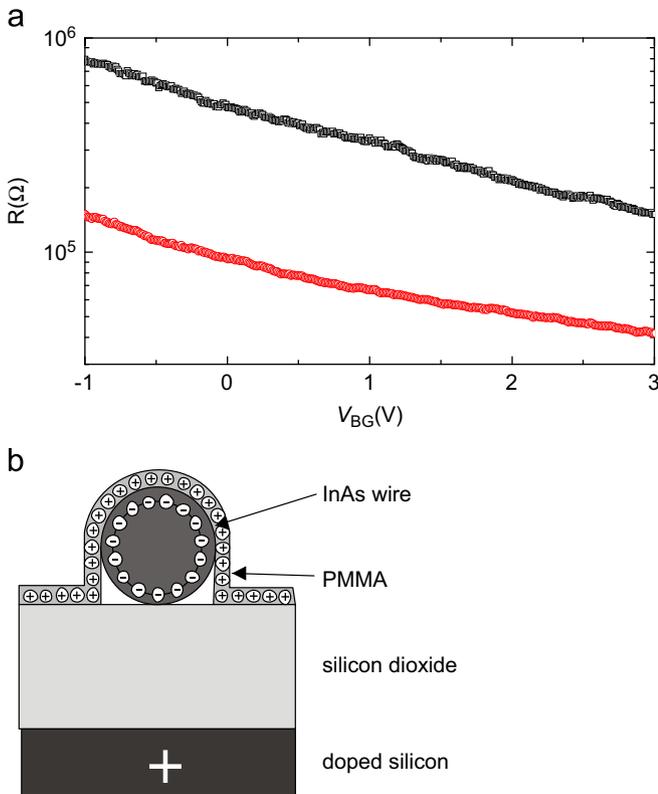


Fig. 6. (a) Resistance of the InAs nanowire vs back-gate voltage. The first curve (open circles) is measured after tip scanning with $V_t = -1$ V and the second curve (open squares) after tip scanning with -2 V. (b) Schematic illustration of the charge distribution in the InAs nanowire sample covered with PMMA.

applied not only to change the potential of a tube or a nanowire as a whole similar to a back-gate but also allows to configure the Coulomb potential along the 1D sample. An example of such application for investigation of local conductance of the InAs wire is presented in the next section.

Fig. 7 shows the topography of the InAs wire with a length of $1.9 \mu\text{m}$ and a diameter of 100 nm . Fig. 7b–d shows Kelvin probe scans made after long scanning with tip potential of 0 V (configuration I), after five line scans across the wire to form local positively charged region with tip voltage of 3 V (configuration II), and after five line scans across the wire $V_t = -3$ V (configuration III), respectively. The resulting potential profiles along the wire, excluding regions nearby the contact pads, are depicted in Fig. 8. Coordinate denotes distance from edge of the top contact pad. Curves (a) open squares, (b) open triangles and (c) open circles relate to configurations I, II and III, respectively. While curve (b) demonstrates maximum at $X = 1.1 \mu\text{m}$, curves (a) and (c) are more flat and are close to be the same. Thus, the final scanning with a tip voltage of $V_t = -3$ V restores the initial potential profile almost completely. The only difference is some depletion of the region near by the bottom contact.

Fig. 9 presents the resistance of the wire vs back-gate voltage measured in these three conditions. Curves (a)–(c) are related to Fig. 7b–d. At positive back-gate voltages the measured difference of the wire resistance for configuration I and II is around $\Delta R_M \approx 2.2 \text{ k}\Omega$ (see curves (a) and (b), Fig. 9). It is possible to calculate this resistance difference by assuming that the wire is homogeneous and the slope of curve (a) (dR/dV_{BG}) is constant: $\Delta R_C = (C_{C-W}/C_{C-BG})\kappa \int_0^l \Delta U(x) dx = 2.7 \text{ k}\Omega$. Here l is the wire length, $\kappa = (1/l)(dR/dV_{BG}) = -0.7 \Omega/\mu\text{m}$ is the normalized response of the resistance on the deviation of the back-gate

voltage, and $\Delta U(x)$ is the measured difference between the potentials of configurations I and II (see Fig. 8). The integration is performed along the wire length. The calculated value ΔR_C is close to the measured one ΔR_M . Therefore we can conclude that the wire is quite homogeneous. Namely, κ is constant along the wire and its value does not depend strongly on back gate voltage as well. The same calculation can be performed for configurations I and III and results in $\Delta R_C = 0.5 \text{ k}\Omega$. This value is close to the measured resistance values at $V_{BG} > 1$ (see Fig. 9). At low back-gate voltages $V_{BG} < 0$ V the situation changes dramatically. The difference between the values of wire resistance for configurations I and III is more than $2 \text{ k}\Omega$ revealing that the InAs wire is not homogeneous any more and even quite small potential profile variation along the wire results in a significant difference in the conductance when the electronic system is depleted pointing bottom contact pad to wire interface as a region with potential barrier.

As it was mentioned previously the induced potential increases gradually from scan to scan. This effect can be used for another type of measurements to investigate the local conductivity of the wire. This “charging gate imaging” method is based on the standard scanning gate technique of mapping the wire resistance while a charged tip scans the sample area. However, in this case only the profile along the slow area scanning direction contains data of interest and it is proper to align this coordinate close to parallel to the wire/tube axis. Thus, even scanning an area effectively results in a 1D data array. The measured profile resembles the standard cut of scanning gate image integrated along the slow scanning direction because of PMMA charging.

A topography image (a) and a charging gate image (b) of a InAs wire are presented in Fig. 10. The potential of the surface was flatted by numerous scans with zero tip voltage and the image (b) is the first scan with $V_t = -2$ V. The slow coordinate is X and the scanning goes from left to right. It is clearly visible that resistance of the wire starts to increase when tip reaches the left end of the wire ($X = 4.3 \mu\text{m}$) and saturates at $X = 5.9 \mu\text{m}$ which is the right end of the wire. The resistance of the wire stays constant outside this region.

Three curves of charging gate images made with $V_t = -2$ V are presented in Fig. 11. Open squares (a) is the first scan (see Fig. 10b), solid circles (b) is the cut of twentieth scan (curve is multiplied by 2 for convenience) and solid squares (c) is the cut of fortieth scan. It is clearly visible that the behavior of the wire resistance vs tip position significantly changes, see curves (a) and (c) of Fig. 11. Not only the resistance value increases by a factor of 5 but the shape of the curve is changed as well. While in curve (a) the slope close to the contact pads is twice as steep as in the center region of the curve, in the curve (c) slope approximately changes by a factor of 10. The steepness of the slope reflects the profile of the conductance valley namely the large slope reflects the presence of a potential barrier. This barrier presumably comes from contamination atoms at the wire to metallic contact interface. This interpretation is similar to one used for scanning gate image interpretation [22] keeping in mind that the scanning gate image profile is close to dR/dx in this experiment.

According to the measured experimental data we can conclude that at high electron densities in the nanowire the potential barrier at the wire to contact pads interfaces is screened. However, when the electron density is decreased no more screening occurs so that the interface barrier starts to play a dominant role by governing the wire resistance. We attribute the presence of this barrier to the moderate quality of the contacts themselves. The same behavior was obtained on another two samples at room temperature. These results confirm one obtained in previous section revealed potential barrier in the wire to metallic contact

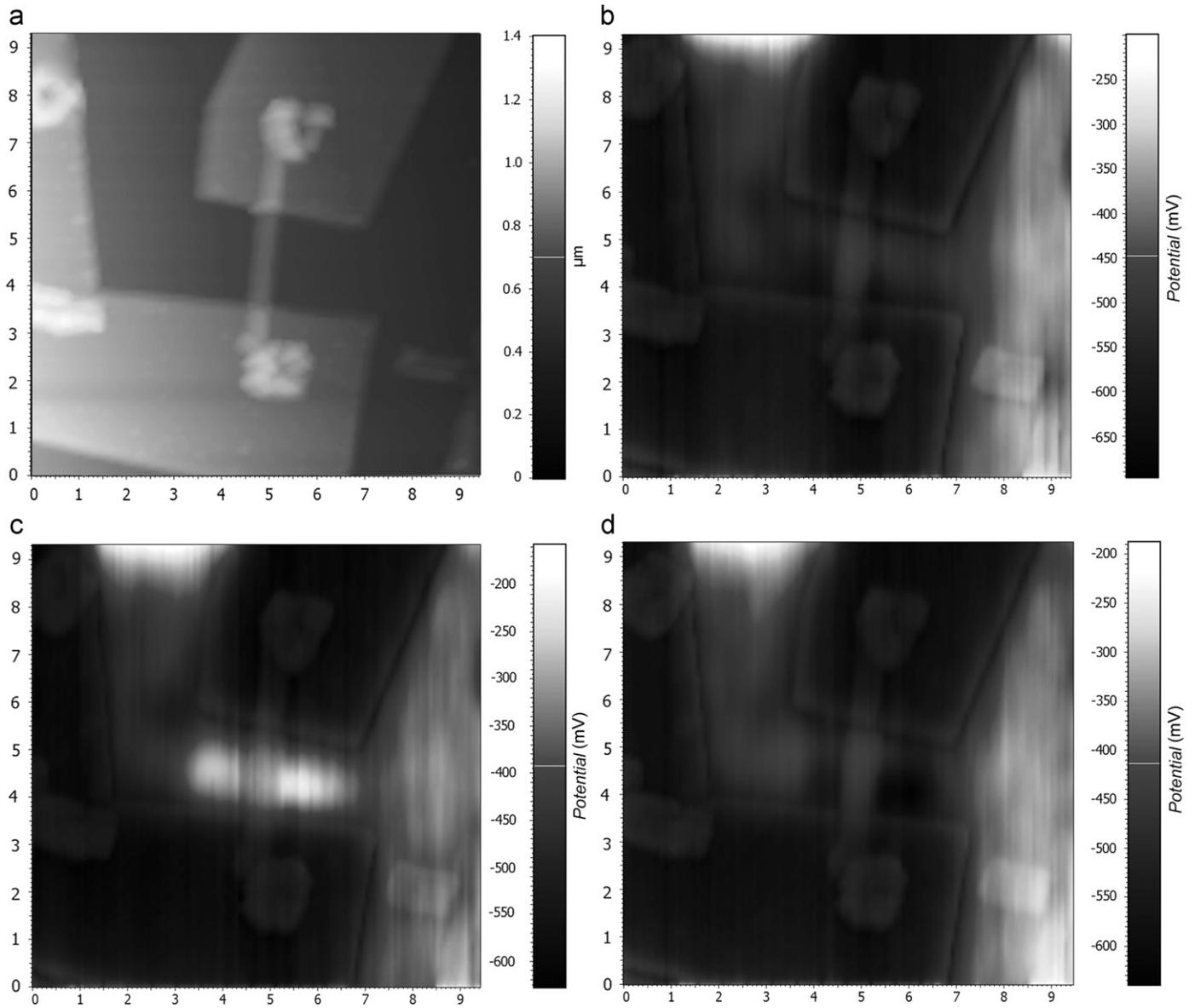


Fig. 7. (a) Topography image of an InAs wire made with AFM. (b)–(d) Kelvin probe mappings of the surface potential after (b) several scanning with $V_t = 0$ V, (c) line scanning with $V_t = +3$ V across the wire and (d) line scanning with $V_t = -3$ V across the wire.

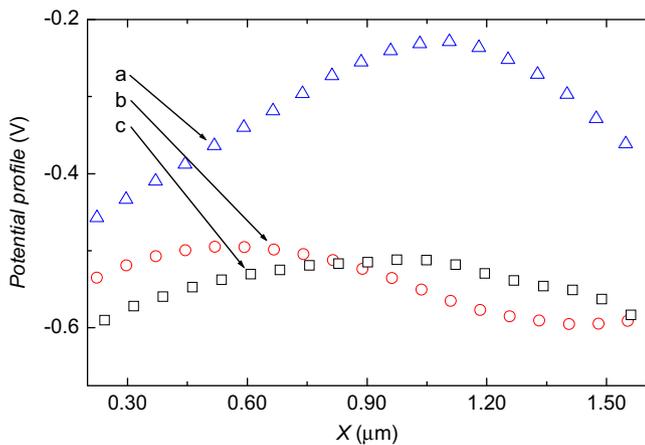


Fig. 8. Potential profile along the InAs nanowire after (a) several scanning with $V_t = 0$ V (open squares), (b) line scanning with $V_t = +3$ V across the wire (open triangles) and (c) line scanning with $V_t = -3$ V across the wire (open circles). After the line scanning with a tip voltage of -3 V the potential profile along the nanowire is almost restored.

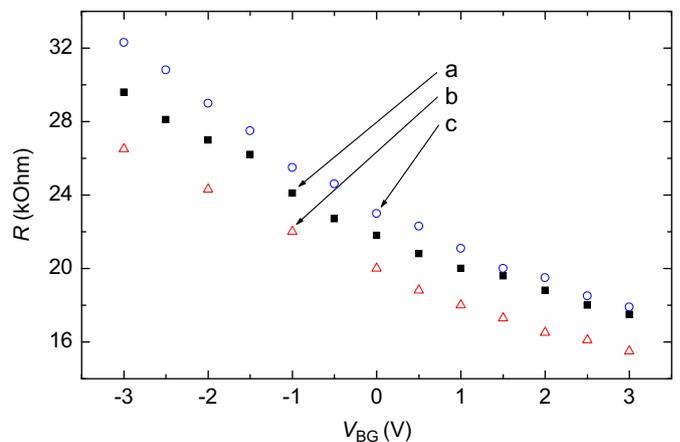


Fig. 9. InAs nanowire vs back-gate voltage after (a) several scanning with $V_t = 0$ V (open squares), (b) line scanning with $V_t = +3$ V across the wire (open triangles) and (c) line scanning with $V_t = -3$ V across the wire (open circles).

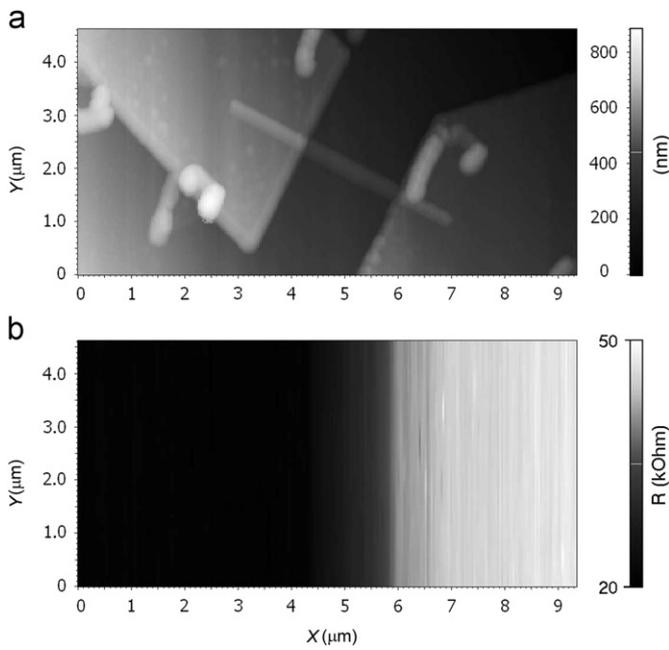


Fig. 10. (a) Topography image of InAs wire made with an AFM. (b) First charging gate image made with $V_t = -2$ V after several scans with tip voltage of $V_t = 0$ V. The slow scanning direction is X.

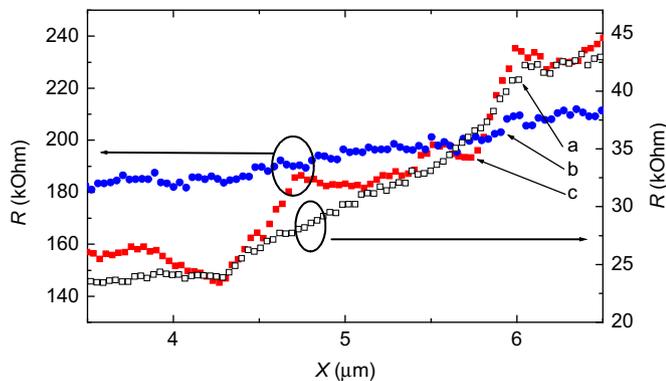


Fig. 11. Profiles of charging gate images made with $V_t = -2$ V dedicated to the first scan: open squares (a), solid circles (b) is the cut of twentieth scan (curve is multiplied by 2 for convenience) and solid squares (c) is the cut of fortieth scan. The steepness of the slope reflects the profile of conductance valley, i.e. the large slope corresponds to the presence of a potential barrier.

interface region. These barriers in an InAs wires have been observed previously [15,23].

4. Conclusions

In conclusion, we presented a new technique to create a reconfigurable Coulomb potential with a charged AFM tip using a residual PMMA layer for charge accumulation. By using this method a induced surface potential shift of about 2 V with a characteristic decay time of 15 min can be obtained. The achievable potential gradient is approximately 1 V/ μm . The large mutual capacitance between the induced charges and electrons

in 1D structure $C_{W-C}/C_{W-BG} \approx 13$ proves that the introduced method is very promising for future application concerning electronic transport investigations of low-dimensional structures of micron and submicron sizes.

As a demonstration of the effectiveness of the introduced method for investigations of electronic transport properties of 1D objects, the local conductivity of InAs wires was studied. It could be shown that at $V_{BG} > 0$ the wire is almost homogeneous with a good screening by the electronic system. When a negative back-gate voltage is applied and the electronic system is depleted the wire becomes essentially inhomogeneous. Additionally, when the wire is close to the pinch-off regime and the electronic system is almost depleted the effect of presence of potential barrier near by the contact pad region becomes essential and governs the wire resistance. In the regime far from pinch-off the barriers are screened by the electronic system and their effect on the wire resistance is negligible.

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